REMARKS

This amendment is responsive to the Office Action mailed August 16, 2004. All rejections are respectfully traversed in view of the amendments and remarks herein. Reconsideration is requested.

Claims 1-30 are pending in this application.

Claims 1-9,11-23 and 25-30 stand rejected.

Claims 10 and 24 stand objected to.

Claims 1, 10, 15, 24 and 28-30 are independent.

Claims 1-3, 10, 15-17, 23, and 28-30 are herein amended.

Claims 31 and 32 are herein added.

The Office Action objects to claims 23 and 24 based on an improper dependency. Claim 23 has been herein amended to depend from claim 22.

The Office Action rejects claims 1, 12, 14, 14 and 26 under 35 U.S.C. § 102(e) based on Jourdan, U.S. Patent No. 6,438,673 ('673 hereinafter). The present invention is distinguishable from Jourdan '673, however, because the application includes claims directed to a translation lookaside buffer having page table entries corresponding to a particular processor of a plurality of processors, and identifying page table references indicative of references to common memory locations by a plurality of processors, as disclosed at page 13, lines 15-27.

In further detail, the present application discloses a system for detecting and flagging improper speculative instruction execution using a speculative execution controller coupled to a plurality of translation lookaside buffers, each corresponding to a respective processor. The speculative execution controller detects a match between an access to a page table entry of a first processor and an existing translation lookaside buffer entry of another (e.g., a second processor in which the speculative execution controller operates). The result is a detected multiaccess memory condition that indicates that speculative execution of instructions related to that page (i.e., contained in the page of memory or that

reference data therein) is to be disabled or not allowed. Once the speculative execution controller detects a multiaccess memory condition indicating that the translation lookaside buffer spans of two or more processors overlap, the speculative execution controller sets the speculation indicator of the corresponding page table entry in main memory and can rely on a cache coherency protocol to detect the change to that main memory location and to propagate this change to the cache contents of each processor that references this memory location, as described in the specification at page 14, lines 4-30.

Jourdan '673, on the contrary, discloses an incremental confidence value operable for comparison with the predetermined confidence threshold, as the Office Action discusses (Col. 4, lines 33-36). The confidence threshold comparison is a RANGE CHECK based on the entry being GREATER THAN OR EQUAL TO the predetermined threshold (col. 5, lines 7-12). Confidence logic employs the confidence value to generate a confidence indication, and in turn, the confidence logic generates a speculative access indication from the confidence indication (Col. 4, lines 39-50).

Therefore, the present claims include subject matter directed to a system which detects a multiaccess memory condition based on a reference to a memory location common to a plurality of page table entries, in which the page table entries each corresponding to at least a first processor and a second processor, and setting a value of the speculation indicator based on the multiaccess memory condition to indicate that speculative execution of instructions by at least one of the first and the second processors is not allowed in the computerized device for instructions that reference the memory location. Jourdan '673 employs an incremental confidence value operable for comparison with the predetermined confidence threshold, rather than a reference to a memory location common to a plurality of page table entries.

Accordingly, claims 1 and 15 are herein amended with the subject matter of former claims 2 and 3 to recite that the multiaccess memory condition is based on a reference to a memory location common to a plurality of page table entries,

the page table entries each corresponding to at least a first processor and a second processor, and further that setting value of the speculation indicator is to indicate that speculative execution of instructions by at least one of the first and the second processors is not allowed in the computerized device for instructions that reference the memory location, to further clarify and distinguish the claimed invention.

In this regard, claims 2 and 3 have been similarly amended to clarify the first and second processors and the memory location common to a plurality of (i.e. first and second processor entries) page table entries. Further, independent claim 15 and dependent claims 16 and 17 have been similarly amended with respect to the claimed processor configuration. As the limitations now recited in amended claims 1 and 15 represent subject matter previously claimed in dependent claims 2 & 3, and 16 & 17 respectively, it is submitted that no new search is required.

Accordingly, it is respectfully submitted that Jourdan '673 does not anticipate invention claimed in presently amended claims 1 and 15 because Jourdan does not show, teach, or disclose detecting a multiaccess memory condition based on a reference to a memory location common to a plurality of page table entries, the page table entries each corresponding to at least a first processor and a second processor, and further setting value of the speculation indicator to indicate that speculative execution of instructions by at least one of the first and the second processors is not allowed in the computerized device for instructions that reference the memory location, as recited in amended claims 1 and 15.

The Office Action indicates that claims 10 and 24 are objected to as depending from a rejected base claim, but allowable in other respects. Accordingly, claims 10 and 24 have been herein amended in independent form to recite the features of the claims from which they depend. Further, claims 31 and 32 have been herein added to reflect the subject matter of former claims 10 and 24 and the amended claims 1 and 15, respectively.

Independent claims 28-30 have been amended similarly to claims 1 and 15, and are respectfully submitted as allowable for the reasons given above with respect to claims 1 and 15. Further, as the remaining claims depend from, either directly or indirectly, from claims 1 and 15, it is respectfully submitted that these claims are also in condition for allowance.

Applicant hereby petitions for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-0901.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 366-9600, in Westborough, Massachusetts.

Respectfully submitted,

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